

Low-Power-Consumption Integrated Tunable Filters for WDM Switching Applications in Silicon Photonics

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Abstract—We present the experimental results of thermally tunable double microring resonator devices for integrated wavelength division multiplexing applications. The devices demonstrated a free-spectral range up to 2.4 THz (19.2 nm) around 1550 nm and a channel rejection higher than 35 dB. Using Ti/TiN metal heaters, a power consumption of 20 mW per FSR per ring is achieved, which outperformed analogous devices fabricated using the standard silicon process. A thermal tuning efficiency of 0.95 nm/mW is accomplished, and a symmetric tuning is obtained with less than 1% of electrical compensation.

Index Terms—Integrated optics, optical switches, ring resonators.

I. INTRODUCTION

IN THE last decade integrated switching fabrics have attracted a significant interest because of their potential application for scalable on-chip interconnections. In this context, special attention has been devoted to silicon photonic solutions due to their CMOS compatibility, integration, scalability and low power consumption [1].

For wavelength-dependent switches, ring resonators are usually considered as the key building block because of their high frequency selectivity and small footprint [2]–[4]. However,

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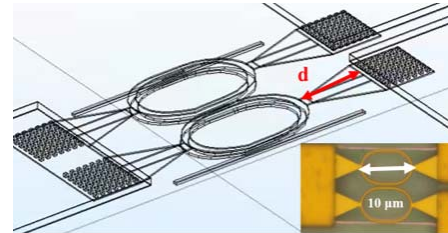


Fig. 1. Schematic representation of the coupled rings under investigation (left) and microscope picture of the same device (right).

their performance can be limited in terms of neighbor channel rejection [5], [6], pass-band flatness and filter roll-off. For those reasons, higher-order ring-based filters represent a more suitable solution for wavelength division multiplexing (WDM) switching applications [7]–[10]. Nevertheless, most of the previous results are characterized by a small free spectral range (FSR) or a limited channel rejection [11]–[13]. In our previous work [14], we described the design procedure and the successful experimental demonstration of second order microring filters, based on modified racetrack resonators obtained with Bezier bends. The final device is characterized by a FSR of 2.4 THz and a 3dB bandwidth of about 100GHz (0.8 nm), while thermal tuning is obtained by using silicon-integrated heaters located inside the rings. In this letter, we present a different heating strategy using metallic heaters that provide higher power efficiencies (20mW/FSR/ring) and improve the symmetrical heating with less than 1% of power difference required for perfect spectral alignment. Furthermore, a detailed optical characterization, including loss measurements in *off* state, statistical data with a full switching array, and a description of inter-die resonance variability is presented.

II. DESIGN AND SIMULATION

The resonator devices are modeled and designed by using the transfer matrix method reported in [14]. The structure of the second-order micro-ring filter based on modified racetrack resonators and Bezier bends is illustrated in Fig. 1.

The design of the racetrack perimeter and coupling coefficient are determined by the FSR and the transmission bandwidth required for a WDM system as described in [14]. The Ti/TiN metal layer used for the metallic heater exhibits a uniform sheet resistance of $6.3 \pm 0.3 \Omega/\text{square}$ and is 120 nm thick. The width of the metal heater tracks is set to

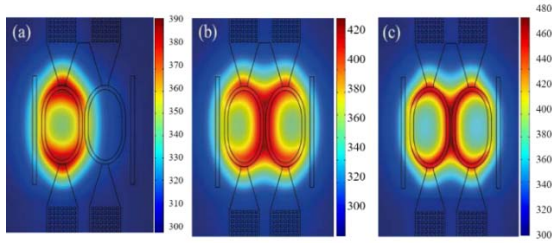


Fig. 2. Temperature distribution (K) of the heat propagation along the silicon waveguide for the applied voltage $V = 1V$ on one single heater (a) and for the applied voltage of 1V on the two heaters on the silicon waveguide plane (b) and on the heaters plane (c).

434 nm in order to achieve a target resistance of $\sim 200 \Omega$ needed for low-driving voltage electronic control [1]. The thermal performance of the device is computed with a 3D thermo-electrical simulation following the approach presented in [15]. Using a thermo-optic coefficient of $1.8 \cdot 10^{-4} \text{ RIU/K}^{-1}$, a tuning efficiency of 21.2 mW/FSR/ring is calculated. To evaluate the contribution of a single heater, we simulate the temperature distribution in the device when only one heater is operating as shown in Fig. 2(a). In this condition, an increment in the average temperature of 40 K in the non-heated racetrack is observed. The benefit of two heaters is clearer when both heaters are working. In this case, the temperature in the racetrack underneath is 30 K higher than in the case when only one heater is working. Fig. 2(b) and Fig. 2(c) describe the temperature distribution at the silicon level and at the metal level, respectively, showing that the temperature difference between the racetracks and the heaters is about 60 K.

III. FABRICATION AND PERFORMANCE

The device was fabricated at CEA-LETI on an 8" silicon-on-insulator (SOI) wafer with $2 \mu\text{m}$ buried oxide and 220 nm silicon layer. The first step of the fabrication process is a deep ultra-violet 193 nm optical lithography printing and the silicon layer is then patterned by reactive-ion-etching (RIE). Single polarization grating couplers with a shallow-etch depth of 70 nm are used for optical access to the input, through and drop ports of the ring-based filter. As shown in Fig. 1, the metallic layer is separated from the silicon waveguide by a 600 nm-thick silica layer. The heater consists in a double layer made of Ti/TiN obtained after the deposition of 110 nm thick titanium nitride on 10 nm of titanium. Eventually, the metal heaters are coated by 320 nm-thick silica cladding. The optical characterization of the proposed device, performed by the independent thermal tuning of the two devices with three testing probes and a common ground, demonstrates that the system requirements for a WDM switching application are fully satisfied, i.e. maximum extinction ratio of 35 dB and a 200-GHz channel rejection of 20 dB [1].

Figs. 3 and 4 report the thermal tuning performance of the device, where an applied voltage of 1V induces a red shift of half FSR. These results are achieved by symmetrically heating the two rings. The zoom in Fig. 3 (b) clearly shows that applying a voltage difference of less than 100 mV compensates the slight asymmetry of less than 1 dB in the

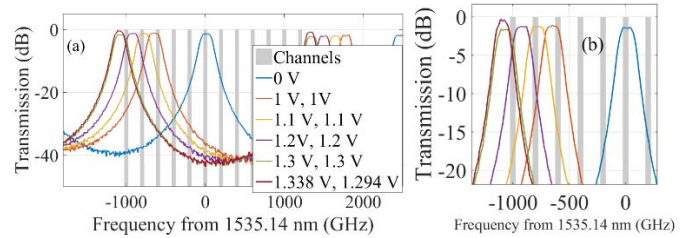


Fig. 3. (a) Spectral shift due to thermal tuning for the coupled ring with $d = 7 \mu\text{m}$; (b) Zoom of the thermal tuning characteristic. The voltage values reported correspond to those applied to the two heaters.

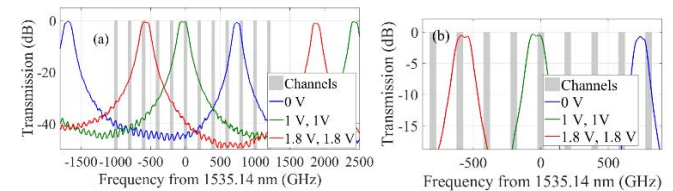


Fig. 4. (a) Spectral shift due to thermal tuning for the coupled ring with $d = 6 \mu\text{m}$; (b) Zoom of the thermal tuning characteristic. The voltage values reported correspond to those applied to the two heaters.

filter shape. Equivalently, as shown in Fig. 4, a symmetric tuning results in a loss of the filter response below 1 dB. The difference between the devices investigated in Figs 3 and 4 is the distance between the ring and the vias (parameter “ d ” in Fig.1) that is equal to $7 \mu\text{m}$ and $6 \mu\text{m}$, respectively. The measured power consumption is 22 mW/FSR/ring (Fig. 3) and 20 mW/FSR/ring (Fig. 4), which are remarkably improved compared to the state of the art of 35 mW/FSR/ring measured in [13] and in excellent agreement with simulation results shown in the previous section, i.e., 21.2 mW/FSR/ring . The efficiency of the metal heater under investigation is superior to the doped silicon heaters reported in [14], which were manufactured inside the ring resonators.

The main reason is due to the area of the racetrack that is exposed to the heater. Indeed, in the doped silicon heater, the heat is transferred through the sidewall of the silicon waveguide, which is 220 nm thick, while in the metal heater case, the heat is transferred through the top surface of the silicon waveguide, which is almost twice, i.e., 410 nm.

Up to a voltage supply of 2.5 V, the heating power reaches 40 mW for the coupled rings, which allows to tune the switch over more than a full FSR (19.2 nm) with a thermal shift efficiency of about 0.95 nm/mW . In Fig. 5 an intensity map of the drop of a double ring structure as a function of the power injected into the top heater (P_{top}) and the bottom heater (P_{bottom}) is given.

This map was obtained by measuring the intensity at a fixed wavelength slightly out of resonance. The 1-dB zone of the curve is centered for both heaters at around 6 mW and the slopes of the dashed lines in Fig. 5 clearly points out the effect of thermal crosstalk between both rings, responsible of the improvement of the tuning efficiency per ring. In order to compare the performance of our device with those reported in the literature, the most relevant results for thermally tunable ring resonators are summarized in Table I. The two main approaches for integrated heaters are: metallic heater on the top of the silicon ([16]–[21]) and doped silicon

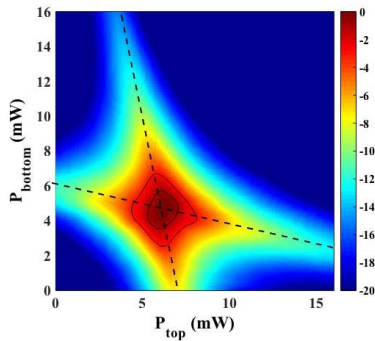


Fig. 5. Power Intensity map in dB of the Drop of a double ring as a function of the power injected into the top and bottom heater obtained at a fix wavelength. The inner contour plots represent the zone within 1 dB and 3 dB of the maximum power, respectively. The dash lines are guides for the eye following the peaks of each of the ring resonances.

TABLE I
TUNING POWER OF STATE OF THE ART THERMALLY
TUNED SILICON MICROCAVITIES

Ref.	Device type	Power per FSR per ring (mW)	Features
[10]	Double-ring	50	Doped silicon
[14]	Double ring	37	Doped silicon
[15]	Single-ring	21	metallic
[16]	Single-ring	105	metallic
[17]	Single-ring	35	metallic
[18]	Cascade rings	89	metallic
[19]	Single-ring	20	Doped silicon
[20]	Single-ring	56	Multi-wire metallic
[22]	Single ring	3.9	Local substrate removal
[23]	Single-ring	2.4	Metallic, substrate-removal
[24]	Double ring	30	Metallic, undercut
This work	Double ring	20	Metallic heater

heaters ([10], [14], [22]). The thermal efficiency can be further improved by local substrate removal [23] or undercut structures [24]. Despite being characterized by an ultra-low tuning power, the devices presented in [22]–[24] require a non-standard substrate-removal processes, which are not available in the majority of multi project wafer foundries. Moreover, with these approaches, the temporal response increases by 10-100 times, which is not suitable for fast-switching applications.

As shown in the table, majority of the published results refers to single ring devices which do not provide high channel rejection as required in WDM switching applications. In the restricted analysis of double ring filters, our devices, with a tuning power of 20 mW/FSR/ring, demonstrate, to the best of our knowledge, the most efficient thermal switches using standard silicon photonic fabrication processes. These features make our proposed integrated device extremely attractive for WDM applications; the collective tuning of the two micro-ring significantly simplifies the electronic control of large switching matrices making the switch suitable for applications that require small footprint and low power consumption.

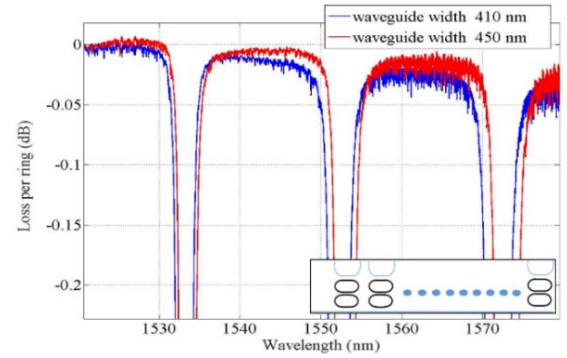


Fig. 6. Loss per ring through 50 identical rings in series. The measurement proves that the loss under off-resonance condition is well below 0.1dB.

IV. SYSTEM-LEVEL ANALYSIS

Considering the final reconfigurable add and drop multiplexer (ROADM) system described in [1], an analysis of the device performance correlated to losses, resonance position and fabrication inaccuracy is performed. One critical parameter in scalable switching fabrics is the switch loss in the off-state. In particular, by using a cross-bar configuration, the light travels through only one switch in *on* state, but many (tens or even hundreds) in *off* state [1], [4]. This requires an extremely low insertion loss between the *input* and the *through* port when the racetrack is out of resonance. In order to characterize such loss values, 50 identical switches have been set in series. The separation is randomly varied to avoid coherent effects. The results are shown in Fig. 6, where the measured non tuned loss has been normalized with the grating coupler response and divided by 50 to obtain the loss per switch. It is obvious for both designs that the loss is lower than 0.05dB in the out-of-resonance regions.

On the other hand, deviations from the nominal SOI thickness and waveguide width generate variations in the resonance precise wavelength [25]. In particular, we have calculated that for the silicon waveguide cross-section used in this work (i.e., 410 nm \times 220 nm) an error of 1 nm in the waveguide thickness produces a 1.35 nm (168.6 GHz) shift in the resonance wavelength at around 1550 nm, while a variation of 1 nm in the waveguide width yields a 0.980 nm (122.5 GHz) resonance shift [26]. While SOI wafers have typical silicon thickness variations of a few nm over the full wafer, on the other hand the waveguide width variations can be much larger. As an example, a variation of up to 15 nm in the waveguide width over the wafer is measured in [27]. Fabrication errors, once calibrated, can be compensated by varying the UV exposure within the wafer. In Fig. 7, we can see that a resonance red-shift of up to 5 nm is measured as we approach the center of the wafer.

However, within a single chip, the variations are much smaller. Each direction of the ROADM in [1] supports 12 channels which are 200 GHz spaced that can be independently added or dropped from the network. Fig. 8 shows the transmission spectra from the non-tuned drop port of the 12 WDM channels of [1], where the wavelength fluctuations are smaller than 75 GHz (0.6 nm) in all cases. In order to generate this grid, the straight part of the racetrack was

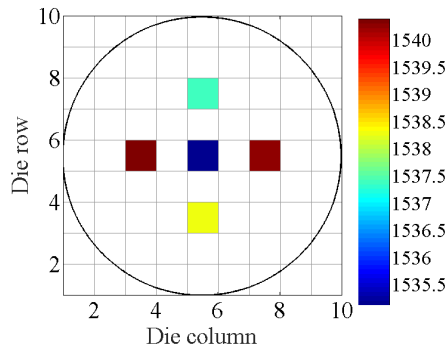


Fig. 7. Spectrum red-shift of the central resonance wavelength of the coupled rings when going from border to center.

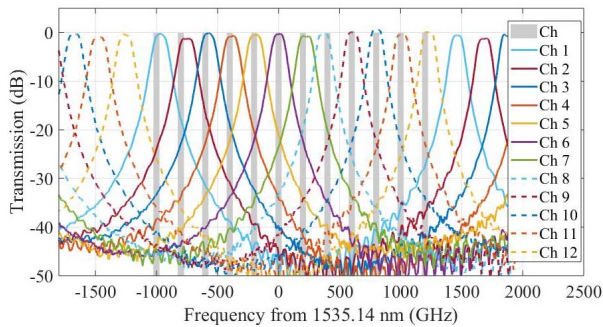


Fig. 8. Drop spectrum of a 12 WDM matrix as a preliminary test.

modified while the Bezier bends were maintained with the same geometry. In this case, the physical separation between switches was $100 \mu\text{m}$. As shown in Fig. 8, indeed, the FSR and the inter-channel distance is well maintained together with a channel isolation at 200 GHz of about 20 dB and a good alignment between channels.

V. CONCLUSIONS

We have presented and experimentally demonstrated a large FSR and low power switching element based on double ring resonators with a record value of power consumption of 20 mW/FSR/ring fabricated using a standard silicon process. The device requires a very low electrical compensation for optimal operation. The thermal and optical performance of the investigated device are suitable for WDM applications, and the low-driving voltage for fully FSR tuning makes it compatible with integrated electronics.

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